What is claimed is:

1. A method of generating a start of packet synchronization sequence for use in a transmitter, said method comprising the steps of:

generating a plurality of N symbols to be transmitted in said synchronization sequence;

generating N-1 predetermined signals;

inserting one of said N-1 predetermined signals after each of the first N-1 symbols in said synchronization sequence; and

wherein N is a positive integer.

2. The method according to claim 1, wherein said predetermined signals comprise time delays or transmitting gaps.

3. The method according to claim 1, wherein N equals seven.

4. The method according to claim 1, wherein said N-1 predetermined signals are chosen to yield a synchronization sequence having relatively high auto correlation properties.

5. The method according to claim 1, further comprising generating a plurality of synchronization sequences wherein each synchronization sequence corresponds to a unique set of N-1 predetermined signals comprising time delays, each set of N-1 time delays chosen so as to minimize the cross correlation between synchronization sequences.

6. The method according to claim 1, further comprising generating a plurality of synchronization sequences wherein each synchronization sequence corresponds to a different packet type.

7. The method according to claim 1, wherein said each symbol comprises a zero shifted code shift keying modulated symbol.

8. The method according to claim 1, wherein said method is implemented in an Application Specific Integrated Circuit (ASIC).

9. The method according to claim 1, wherein said method is implemented in a Field Programmable Gate Array (FPGA).

10. A method of generating a start of packet synchronization sequence for use in a code shift keying (CSK) based transmitter, said method comprising the steps of:

generating a plurality of symbols of known shift rotation to be transmitted in said synchronization sequence;

inserting a predetermined time delay between each of said symbols; and

wherein said predetermined time delays inserted between said symbols define a unique synchronization sequence gap template.

11. The method according to claim 10, wherein said predetermined time delays are chosen to yield a synchronization sequence having relatively high auto correlation properties.

12. The method according to claim 10, wherein each unique synchronization sequence gap template corresponds to a different packet type.

13. A transmitter for use in a spread spectrum communications system, comprising:

synchronization sequence generator adapted to generate a synchronization sequence, said synchronization sequence representing a plurality of synchronization symbols with predetermined time delays inserted therebetween;

an encoder adapted to determine a shift index to be applied to a spreading waveform, said shift index determined based on said synchronization sequence;

a spreading waveform generator adapted to generate a spreading waveform signal in accordance with said shift index; and

wherein delays between spreading waveform signals are determined by said predetermined time delays in said synchronization sequence.

14. The transmitter according to claim 13, further comprising a synchronization sequence gap memory adapted to store a plurality of synchronization sequences, each synchronization sequence comprising a set of symbols with predefined time delays between each of said symbols.

15. The transmitter according to claim 13, implemented in an Application Specific Integrated Circuit (ASIC).

16. The transmitter according to claim 13, implemented in a Field Programmable Gate Array (FPGA).

17. A communications station for transmitting and receiving signals to and from other stations connected over a shared communications media based network, comprising:

a coupling circuit for generating a receive signal received over said network and for outputting a transmit signal onto said network;

a transmitter adapted to modulate a synchronization sequence and data to be transmitted in accordance with a modulation scheme so as to generate said transmit signal therefrom, wherein said transmitter comprises means for generating a plurality of symbols of known shift rotation to be transmitted in said synchronization sequence and means for inserting a predetermined time delay between each of said symbols;

a receiver adapted to demodulate said receive signal in accordance with said modulation scheme so as to generate a receive data signal therefrom;

a media access control (MAC) circuit adapted to interface an application processor to said shared communications media; and

said application processor adapted to control the operation of said transmitter, receiver and MAC and to provide an interface between said MAC and an external host.

18. The communications station according to claim 17, wherein said first signal comprises a series of time delays in accordance with a synchronization sequence gap template.

19. The communications station according to claim 17, further comprising a synchronization sequence gap memory adapted to store a plurality of synchronization sequences, each synchronization sequence comprising a set of symbols with predefined time delays between each of said symbols.

20. The communications station according to claim 17, wherein said modulation scheme comprises code shift keying (CSK) modulation.

21. The communications station according to claim 17, wherein said transmitter and receiver are implemented in an Application Specific Integrated Circuit (ASIC).

22. The communications station according to claim 17, wherein said transmitter and receiver are implemented in a Field Programmable Gate Array (FPGA).